WHAT IS CLAIMED IS:

1. A non-volatile semiconductor memory device comprising:

a semiconductor substrate; and

a memory cell having a floating gate provided through a tunnel insulating layer on said semiconductor substrate, and a control gate provided through an inter-layer insulting layer on said floating gate,

wherein said inter-insulating layer includes:

a silicon oxide layer contiguous to said floating gate;

a first silicon nitride layer provided by a CVD method on said silicon oxide layer; and

a second silicon nitride layer provided on said first silicon nitride layer and having a lower trap density than that of said first silicon nitride layer.

2. A non-volatile semiconductor memory device according to claim 1, wherein said second silicon nitride layer is formed by carrying, over a surface of said substrate, active Si and N obtained by plasma-decomposing at least a silane-series gas and a gas containing nitrogen.

3. A non-volatile semiconductor memory device according to claim 1, wherein a quantity of hydrogen content of said first silicon nitride layer is $10^{21}/cm^3$ or more.

4. A non-volatile semiconductor memory device according to claim 1, wherein a quantity of hydrogen content of said second silicon nitride layer is $10^{19}/cm^3$ or less.

5. A non-volatile semiconductor memory device comprising:

a semiconductor substrate; and

a memory cell having a floating gate provided through a tunnel insulating layer on said semiconductor substrate, and a control gate provided through an inter-layer insulting layer on said floating gate,

wherein said inter-insulating layer includes:

a silicon oxide layer contiguous to said floating gate; and

a silicon nitride layer deposited on said silicon oxide layer and having a lower trap density than that of said silicon nitride layer formed by a CVD method.

6. A non-volatile semiconductor memory device according to claim 5, wherein said silicon oxide layer is deposited by carrying, over a surface of said substrate, active Si and N obtained by plasma-decomposing at least a silane-series gas and a gas containing nitrogen.

7. A non-volatile semiconductor memory device comprising:

a semiconductor substrate; and

a memory cell having a floating gate provided through a tunnel insulating layer on said semiconductor substrate, and a control gate provided through an inter-layer insulting layer on said floating gate,

wherein said inter-insulating layer includes:

a silicon oxide layer contiguous to said floating gate; and

a silicon oxide layer deposited on said silicon oxide layer and having a quantity of hydrogen content on the order of $10^{19}/cm^3$ or less.

8. A non-volatile semiconductor memory device according to claim 7, wherein said silicon oxide layer is deposited by carrying, over a surface of said substrate, active Si and N obtained by plasma-decomposing at least a silane-series gas and a gas containing nitrogen.

9. A non-volatile semiconductor memory device comprising:

a semiconductor substrate; and

a memory cell having a floating gate provided through a tunnel insulating layer on said semiconductor substrate, and a control gate provided through an inter-layer insulting layer on said floating gate,

wherein said inter-insulating layer includes:

a silicon oxide layer serving as a layer contiguous to at least one of said floating gate and said control gate, and having a lower trap density than that of a silicon nitride layer formed by a CVD method.

10. A non-volatile semiconductor memory device according to claim 9, wherein said silicon nitride layer is formed by carrying, over a surface of said substrate, active Si and N obtained by plasma-decomposing at least a silane-series gas and a gas containing nitrogen.

11. A non-volatile semiconductor memory device according to claim 9, wherein said silicon nitride layers are so double-layered as to be contiguous to both of said floating gate and said control gate, and

a silicon oxide layer is interposed in between said double-layered silicon nitride layers.

12. A non-volatile semiconductor memory device according to claim 9, wherein said silicon nitride layers are so double-layered as to be contiguous to both of said floating gate and said control gate, and

a stacked layer consisting of a silicon oxide layer and a silicon nitride layer formed by a CVD method is interposed in between said double-layered silicon nitride layers.

13. A non-volatile semiconductor memory device

according to claim 9, wherein said silicon nitride layer is provided only on the side contiguous to said floating gate, and

a silicon oxide layer and a stacked layer consisting of a silicon nitride layer and a silicon oxide layer which are formed by the CVD method, are provided on said silicon nitride layer.

14. A non-volatile semiconductor memory device comprising:

a semiconductor substrate; and

a memory cell having a floating gate provided through a tunnel insulating layer on said semiconductor substrate, and a control gate provided through an inter-layer insulting layer on said floating gate,

wherein said inter-insulating layer includes:

a silicon oxide layer serving as a layer contiguous to at least one of said floating gate and said control gate, and having a quantity of hydrogen content on the order of $10^{19}/cm^3$ or less.

15. A non-volatile semiconductor memory device according to claim 14, wherein said silicon nitride layer is formed by carrying, over a surface of said substrate, active Si and N obtained by plasma-decomposing at least a silane-series gas and a gas containing nitrogen.

16. A non-volatile semiconductor memory device according to claim 14, wherein said silicon nitride layers are so double-layered as to be contiguous to both of said floating gate and said control gate, and

a silicon oxide layer is interposed in between said double-layered silicon nitride layers.

17. A non-volatile semiconductor memory device according to claim 14, wherein said silicon nitride layers are so double-layered as to be contiguous to both of said

floating gate and said control gate, and

a stacked layer consisting of a silicon oxide layer and a silicon nitride layer formed by a CVD method is interposed in between said double-layered silicon nitride layers.

18. A non-volatile semiconductor memory device according to claim 14, wherein said silicon nitride layer is provided only on the side contiguous to said floating gate, and

a silicon oxide layer and a stacked layer consisting of a silicon nitride layer and a silicon oxide layer which are formed by the CVD method, are provided on said silicon nitride layer.